REMARKS/ARGUMENTS

Reconsideration of the application is respectfully requested for the following reasons:

The present remarks are in response to the Office Action mailed September 20, 2006, in which Claims 1-26 were rejected. Claims 1 and 20 have been amended in this application, and Claim 19 is canceled. No claims are added. Therefore, Claims 1-18 and 20-26 remain in this application.

Applicants respectfully request reconsideration in light of the following remarks.

CLAIM REJECTIONS- 35 U.S.C. SECTION 102(b)

Claims 1 and 5-7 stand rejected under 35 U.S.C. 102(b) as being anticipated by Lee et al. (U.S. Patent No. 6,033,981).

Lee et al. '981 provides a keyhole-free process for high aspect ratio gap filling, which includes follow steps: providing a substrate (10) having several conductive lines (12) (see Fig. 3), forming a first HDP oxide layer (14) on the substrate (10) and the conductive lines (12) (see Fig. 4), etching the first HDP oxide layer (14) to expose the sidewalls of the conductive lines (12) but the first HDP oxide layer (14) still cover the top of the conductive lines (12) (see Fig. 5), depositing a silicon nitride layer (16) on the substrate (10) and the conductive lines (12) (Fig. 6), the CMP polishing to remove part of the silicon nitride layer (16) for exposing the first HDP oxide layer (14) on the top of the conductive lines (12), the oxide and nitride dip for remove the silicon nitride layer (16) and the first HDP oxide layer (14) on the top of the conductive lines (12) (Fig. 8), forming silicon nitride spacers (20) (see Fig. 9), and depositing a second HDP oxide layer (22) to fill gap without voids (see Fig. 11).

The Examiner is of the opinion that the Fig. 2-5 and 13 of Lee et al. '981 disclose all features of the present invention recited in Claims 1 and 5-7. Fig. 2-5 and

13 of Lee et al. '981 disclosed a keyhole-free process for high aspect ratio gap filling, which includes providing a substrate (10) having several conductive lines (12) (see Fig. 3), forming a first HDP oxide layer (14) (see Fig. 4), etching the first HDP oxide layer (14) to expose the sidewalls of the conductive lines (12) (see Fig. 5), forming silicon nitride spacers (20) (see Fig. 9 and 13), and forming a second HDP oxide layer (22) to fill gap without voids (see Fig. 13). Although this process eliminates the nitride deposition (Fig. 6) step, the CMP polishing (Fig. 7), and the oxide and nitride dip (Fig. 8), but it keeps the silicon nitride spacer deposition (Fig. 9) step to form the spacers (20) on the sidewalls of the conductive lines (12) and the spacers (20) is used to form a self-aligned contact between narrowly spaced conducting lines. However, the method for gap filling between metal-metal lines provided by the present invention just includes a first dielectric layer deposition step, removing the first dielectric layer to expose the sidewalls and a second dielectric layer deposition step. It doesn't need or include a spacers deposition step. Thus, the method of the present invention is simpler than the process of Lee et al. '981, and they are different. Therefore, claim 1 is patentable over the cited reference.

Besides, all steps recited in Claim 1 of the present invention are performed in situ in a chamber. There are two kinds of keyhole-free processes for high aspect ratio gap filling are disclosed by Lee et al. '981. One includes nitride deposition (Fig. 6) step, the CMP polishing (Fig. 7), and the oxide and nitride dip (Fig. 8), but the other doesn't. Both of the two processes include a spacers deposition step. No matter the nitride deposition (Fig. 6) step, the CMP polishing (Fig. 7), and the oxide and nitride dip (Fig. 8) or the spacers deposition (Fig. 9) step can be performed in situ in a chamber because they need to be performed by different apparatuses. And both of two processes disclosed by Lee et al. '981 need one or more above-mentioned steps. Thus, the steps of the processes of Lee et al. '981 need to be performed by different apparatuses and teach away form the present invention because of it. Therefore, Lee et al. '981 does not disclose and teach the feature of the present invention and claim 1 is thus patentable over the cited reference. Further claims 5 – 7 are patentable at least by virtue of their dependency to claim 1.

CLAIM REJECTIONS- 35 U.S.C. SECTION 103(a)

Claims 2-4 and 8-26 are stand rejected under 35 U.S.C. 103(a), as being unpatentable over Lee et al. (U.S. Patent No. 6,033,981) as applied to claim 1 and 5-7 in view of Kim et al. (U.S. Patent Application Publication No. 2004/0119170) and Lee et al. (U.S. Patent No. 6,103,630).

Kim et al. provides a semiconductor device having self-contact plug and method for fabricating the same. The semiconductor device has a substrate having cell pads on it and a insulating layer covering the substrate and the cell pads, a conductive layer on the insulating layer and a capping layer on the conductive layer, a first interlayer insulating layer deposited on the insulating layer covering the conductive layer and part of the capping layer, and several spacers on the exposing sidewalls of the cell layer. First, a substrate having cell pads on it and an insulating layer covering the substrate and the cell pads is provided and then the conductive layer and the capping layer are sequentially formed on the insulating layer. Next, the first interlayer insulating layer is deposited on insulating layer and fills the space between the conductive layers. The first interlayer insulating layer is higher than the conductive pattern but it is lower than the capping layer. And then spacers are formed to cover the exposing sidewalls of the capping layer. Finally, the second interlayer insulating layer is formed to cover the first interlayer insulating layer.

Lee et al. '630 provides a new method of etching metal lines using SF_6 gas during the over etch step to present undercutting. A barrier layer, a metal layer and a silicon oxide layer are sequentially deposited on the substrate and cover the semiconductor devices on the substrate. A photoresist mask is formed on the silicon oxide layer. And then the barrier layer and the metal layer are etched away where they are not covered by the photoresist mask. Overetching is performed to remove the barrier layer where it is not covered by the photoresist mask. The SF_6 gas is used to perform the overetching and the fluorine ion from SF_6 gas react with the metal layer and the barrier metal layerto form a passivation layer on the sidewalls of the metal lines for preventing the undercutting of the metal lines.

The Examiner is of the opinion that the features recited in Claims 2-4 and 8-27 have been disclosed and taught by the combination of Lee et al. '981, Kim at al. and Lee et al. '630. However, according to above interpretation about the REJECTIONS-35 U.S.C. SECTION 102(b), Claim 1 is not disclosed and taught by Lee et al. '981 because two features of the present invention are not disclosed and taught. One feature is that the present invention lack the spacer deposition step and makes the method simpler than the process of Lee et al. '981, and another feature is that all steps disclosed in the present invention are performed in situ in a chamber. The two features are also recited in Claim 20 after amendment. Thus, Lee et al. '981 can not disclose and teach all features recited in Claim 20. Besides, Kim at al. (U.S. and Lee et al. '630 does not disclose and teach anything about these two features. So, even Lee et al. '981 are combined with Kim at al. and Lee et al. '630., they can not disclose and teach the two features recited in Claim 1 and 20. Therefore, the rejection of Claim 20 is patentable over the cited references, as are Claims 2-4, 8-18 and 21-26.

Conclusion

Applicants respectfully submit that all pending Claims 1-18 and 20-26 as currently presented are in condition for allowance. Applicants have thoroughly reviewed that art cited but relied upon by the Examiner. Applicants have concluded that these references do not affect the patentability of these claims as currently presented. Accordingly, reconsideration is respectfully requested.

Respectfully submitted,
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